US Patents

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- **6,691,165**: Distributed server cluster for controlling network traffic.

- **6,279,128**: Autonomous system for recognition of patterns formed by stored data during computer memory scrubbing.

- **6,226,683**: Increasing probability multi-stage network.

- **6,128,277**: Reliable array of distributed computing nodes.

- **6,088,330**: Reliable array of distributed computing nodes.

- **6,034,956**: Method of simultaneously attempting parallel path connections in a multi-stage interconnection network.

- **5,890,151**: Method and system for performing partial-sum queries on a data cube.

- **5,835,024**: Multi-stage interconnection network with selectable function switching apparatus.

- **5,778,011**: Method and apparatus for writing and protecting against random and cluster errors in image blocks.

- **5,774,067**: Flash-flooding multi-stage interconnection network with parallel path seeking switching elements.

- **5,734,826**: Variable cyclic redundancy coding method and apparatus for use in a multistage network.
• 5,579,475: Method and means for encoding and rebuilding the data contents of up to two unavailable DASDS in a DASD array using simple non-recursive diagonal and row parity.

• 5,561,805: System for selectively packing together datablocks and efficiently routing independent of network topology in a parallel computer system in accordance with a selected numbering system.

• 5,542,048: Increasing probability multi-stage network.

• 5,513,313: Method for generating hierarchical fault-tolerant mesh architectures.

• 5,461,631: Method for bit resynchronization of code-constrained sequences.

• 5,386,420: Coding method for correction and detection of skewed transitions in parallel asynchronous communication systems.

• 5,357,528: Depth-2 threshold logic circuits for logic and arithmetic functions.

• 5,345,229: Adaptive switching apparatus for multi-stage networks.

• 5,285,454: Method and apparatus for encoding and decoding unordered error correcting codes.

• 5,280,607: Method and apparatus for tolerating faults in mesh architectures.

• 5,280,533: Coding method for skewed transition correction in parallel asynchronous communication systems.

• 5,280,485: Coding method for skewed transition detection in parallel asynchronous communication system.

• 5,271,014: Method and apparatus for a fault-tolerant mesh with spare nodes.